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10/588,638	08/04/2006	Koji Nishikawa	19415-012US1 PCT-05R-205/	9795

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FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
AGUSTIN, PETER VINCENT	
ART UNIT	PAPER NUMBER
2627	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,638	NISHIKAWA, KOJI	
	Examiner	Art Unit	
	Peter Agustin	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-7* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application is a national stage entry (371) of PCT/JP05/03180, filed February 25, 2005.

2. Claims 1-7 are currently pending.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

4. Figures 6 & 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 7 is objected to because of the following informalities:

Claim 7, line 4: "an waveform" should be --a waveform--.

Claim 7, line 7: "one of" should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3 & 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura (US 2003/0137912) in view of Sato et al. (JP 08-307208) (please refer to the machine translation provided by the applicant).

In regard to claim 1, Ogura discloses a waveform equalizer (Figure 1, element 2) comprising: a calculation circuit (paragraph 0079: "high-order ripple filter") that permits free setting of a boost factor by which a gain, in a predetermined frequency range, for an input signal to the waveform equalizer is adjusted and that adjusts the gain for the input signal by varying the boost factor (see paragraph 0079 and the solid line in Figure 2).

In regard to claim 6, Ogura discloses that the calculation circuit is built as an equi-ripple filter (paragraph 0079: "high-order ripple filter").

In regard to claim 7, Ogura discloses an information reproducing apparatus (Figure 1) comprising: a detector (inherent "photodetector" in reproduction means 51) that detects information recorded on a recording medium (50) and that then converts the detected information into an electrical signal ("optical disk reproduction signal"); a waveform equalizer (2) that receives as an input signal thereto the electrical signal; and a processing circuit (13) that processes an output from the waveform equalizer, and the information reproducing apparatus

further comprises a controller (understood from paragraph 0079 and the solid line in Figure 2) that sets the boost factor.

However, Ogura does not disclose: in regard to claim 1, an all-pass filter that is connected to a stage preceding or following the calculation circuit, that has a first conductance amplifier and a second conductance amplifier, and that adjusts and thereby corrects a group delay characteristic of the input signal by varying a conductance of at least one of the first and second conductance amplifiers; in regard to claim 2, that the all-pass filter further has a differentiator that is connected between input and output circuits of the first conductance amplifier and that includes a first capacitor and a second capacitor that is connected between an input side of the first conductance amplifier and an output side of the second conductance amplifier; in regard to claim 3, that an input voltage to the all-pass filter is fed to one input terminal of the first conductance amplifier, a voltage applied to an output terminal of the first conductance amplifier is fed to one input terminal of the second conductance amplifier, a voltage applied to an output terminal of the second conductance amplifier, which voltage corresponds to an output voltage of the all-pass filter, is fed to another input terminal of the first conductance amplifier and to another input terminal of the second conductance amplifier, and the input voltage to the all-pass filter and the voltage applied to the output terminal of the first conductance amplifier have phases inverted relative to each other; in regard to claim 5, that the all-pass filter makes the conductance of the first conductance amplifier variable, and, by varying the conductance of the first conductance amplifier, varies a frequency range in which the group delay characteristic of the input signal is corrected; and in regard to claim 7, a controller that sets whichever of the conductances of the first and second conductance amplifiers is made variable.

Sato et al. disclose: in regard to claim 1, an all-pass filter (Figure 4, APF3) that has a first conductance amplifier (33) and a second conductance amplifier (34), and that adjusts and thereby corrects a group delay characteristic of an input signal by varying a conductance of at least one of the first and second conductance amplifiers (see paragraphs 0035 & 0036); in regard to claim 2, that the all-pass filter (APF3) further has a differentiator (inverter 42 and capacitor C3) that is connected between input and output circuits of the first conductance amplifier (33) and that includes a first capacitor (C3) and a second capacitor (C4) that is connected between an input side of the first conductance amplifier (33) and an output side of the second conductance amplifier (34); in regard to claim 3, that an input voltage (output of APF1) to the all-pass filter (APF3) is fed to one input terminal (+) of the first conductance amplifier (33), a voltage applied to an output terminal of the first conductance amplifier (33) is fed to one input terminal (+) of the second conductance amplifier (34), a voltage (V1) applied to an output terminal of the second conductance amplifier (34), which voltage corresponds to an output voltage (V1) of the all-pass filter (APF3), is fed to another input terminal (-) of the first conductance amplifier (33) and to another input terminal (-) of the second conductance amplifier, and the input voltage to the all-pass filter and the voltage applied to the output terminal of the first conductance amplifier have phases inverted relative to each other (understood from the inverters in APF1 & APF3; note also "phase contrast" in paragraph 0036); in regard to claim 5, that the all-pass filter (APF3) makes the conductance of the first conductance amplifier (33) variable, and, by varying the conductance of the first conductance amplifier, varies a frequency range in which the group delay characteristic of the input signal is corrected (see paragraphs 0035 & 0036); and in regard to claim 7, a controller (inherent component that sets the conductances gm3 or gm4) that sets

whichever of the conductances of the first and second conductance amplifiers (33 & 34) is made variable.

It would have been obvious to one of ordinary skill in the art at the time of invention to have connected the all-pass filter of Sato et al. to the calculation circuit of Ogura, the motivation being to enable phase adjustment with low cost and easy configuration without the need for troublesome compensation (see paragraphs 0019 & 0024).

Allowable Subject Matter

8. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record alone or in combination fails to teach or suggest:

in claim 4, "*wherein the all-pass filter keeps the conductance of the first conductance amplifier constant and makes the conductance of the second conductance amplifier variable, and, by varying the conductance of the second conductance amplifier, adjusts and thereby corrects the group delay characteristic of the input signal while keeping a group delay of the input signal in a direct-current range constant*".

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Suzuki (US 4,817,073) discloses an invention wherein a compensation operation of an equalizer is such that the gain at the low frequency range is boosted by an integration coefficient so as to improve the traceability of the pickup against the eccentricity of the disc.

Kondo et al. (US 5,258,716) disclose an all pass filter having an amplitude characteristic which is flattened with a group delay characteristic thereof being maintained at constant value by adjusting the conductance value of the variable conductance amplifier through adjustment of operating current of the integrator to change its own pole.

Kimura et al. (US 5,463,504) disclose a magnetic disk system and a waveform equalizer consisting of variable conductance amplifiers and capacitors.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter Agustin whose telephone number is (571) 272-7567. The examiner can normally be reached on Monday-Thursday 8:30 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Feild can be reached on (571) 272-4090. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Peter Vincent Agustin/
Patent Examiner, Art Unit 2627